



May 20, 2002

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TECHNOLOGY CENTER 2800

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/076,244 02/13/02

Simon Chooi et al.

A METHOD OF COPPER/COPPER SURFACE
USING A CONDUCTING POLYMER FOR
APPLICATION IN IC CHIP BONDING

Grp. Art Unit: 2813

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.


The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on May 3, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 5/31/02

U.S. Patent 5,923,955 to Wong, "Fine Flip Chip Interconnection", describes a process for creating a flip-chip bonded combination for a first and second integrated circuits using a Ni/Cu/TiN structure.

U.S. Patent 5,891,756 to Erickson, "Process for Converting a Wire Bond Pad to a Flip Chip Solder Bump Pad and Pad Formed Thereby", describes a method for forming a solder bump pad, and specifically to converting a wire bond pad of a surfacemount IC device to a flip-chip solder bump pad such that the IC device can be flip-chip mounted to a substrate.

U.S. Patent 5,795,818 to Marrs, "Integrated Circuit Chip to Substrate Interconnection and Method", describes a method of forming an interconnection between bonding pads on an integrated circuit chip and corresponding bonding contacts on a substrate.

U.S. Patent 5,904,859 to Degani, "Flip Chip Metallization", describes a method for applying under bump metallization (UBM) for solder bump interconnections on interconnection substrates. The UBM comprises a Cu, Cu/Cr, Cr multilayer structure.

CS-99-343C

U.S. Patent 5,767,009 to Yoshida et al., "Structure of Chip on Chip Mounting Preventing from Crosstalk Noise", describes a method of reducing cross talk noise between stacked semiconductor chips by the use of a chip on chip mounting structure.

U.S. Patent 5,804,876 to Lake et al., "Electronic Circuit Bonding Interconnect Component and Flip Chip Interconnect Bond", describes a low contact resistance electrical bonding interconnect having a metal bond pad portion and conductive epoxy portion.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', is written over the printed name.

Stephen B. Ackerman,
Reg. No. 37761

CS-99-343C

10/076,244

Applicant

Simon Chooi et al.

Filing Date

02/13/02

Group Art Unit

2813

**INFORMATION DISCLOSURE CITATION
IN AN APPLICATION**
(Use several sheets if necessary)

JUN 04 2002

PATENT & TRADEMARK OFFICE

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	INDEX DATE & APPROPRIATE
	5923955	7/13/99	Wong	438	108	5/28/98
	5891756	4/6/99	Erickson	438	108	6/27/97
	5795818	8/18/98	Marrs	438	612	12/6/96
	5904859	5/18/99	Degani	216	18	4/2/97
	5767009	6/16/98	Yoshida et al.	438	613	2/10/97
	5804876	9/8/98	Lake et al.	257	737	5/9/97

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.